# DEMO MANUAL DC1950A

## Load Dump Generator

## DESCRIPTION

Demonstration circuit DC1950A generates a load dump pulse for testing 12V and 24V automotive circuits. The output waveform conforms to ISO 7637-2 test pulse 5a, featuring a 2Ω output impedance and automatic adjustment of pulse width as a function of load current. Up to 3A load current is available for testing 12V systems, and up to 1.5A for 24V systems.

In its idling state DC1950A draws no current from its two 9V batteries and as a result, there is no on/off switch. Battery life is approximately 180,000 pulses, limited by the shelf life of the batteries. Only one control is present, a push button which triggers the load dump pulse. Further triggering events are suppressed for approximately 8 seconds to allow the generator adequate cool down time.

Trims for rise time and fall time have been factory pre-adjusted to match the 12V ISO specification.

**Design files for this circuit board are available at http://www.linear.com/demo**



## PERFORMANCE SUMMARY

**Specifications are at $T_A$ = 25°C. 107V INPUT = 107V, 12V INPUT = 14.2V, unless otherwise noted.**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| 107V INPUT | 12V Systems<br>24V Systems | 12.7<br>24.7 | 107<br>209 | 250<br>250 | V<br>V |
| 12V INPUT | 12V Systems<br>24V Systems | 10.7<br>10.7 | 14.2<br>27.7 | 18.7<br>36.7 | V<br>V |
| Output Current Capability | 12V Systems<br>24V Systems | | | 3<br>1.5 | A<br>A |
| Rise Time | Unloaded | | 10 | | ms |
| Pulse Duration, td | Unloaded | | 400 | | ms |

## IMPORTANT CAUTIONS

**DANGER!** High voltage testing shall be performed by qualified personnel only. As a safety precaution at least two people shall be present during high voltage testing.

Do not give or loan DC1950A to a customer. DC1950A is to be used only under the direct supervision of a Linear Technology Field Applications Engineer for purposes of demonstrating LTC products such as surge stoppers and demo boards such as DC1935A, DC2027A and DC2062A.

All personnel in the vicinity of the test set up must wear safety glasses when testing circuits with DC1950A. Cover the DUT to protect against component fragmentation.

If any failure or testing anomaly occurs, immediately turn off the high voltage supply followed by the low voltage supply.

Exercise due caution whenever the high voltage power supply is on. Turn the high voltage supply on just before a test is made, and turn it off as soon as the output pulse is complete.

## IMPORTANT CAUTIONS

If the DUT fails as a low impedance short circuit to ground, M1 and M2 may be destroyed. Because the load dump pulse generator must be capable of delivering high, brief current transients to the DUT (such as might arise from a capacitive load), DC1950A is not current limited. The only protection is current limiting in the high voltage supply and the effect of R17 and R18. If the high voltage supply is heavily bypassed, the energy stored in these capacitors may be sufficient to destroy M1 and M2 as they operate outside of the supply's current limit circuit. As a precaution, perform a series of tests with gradually increasing voltage and current before applying full voltage and full load.

Do not load the output with less than 30Ω. As an example a 4Ω load draws just 3A at 12V, but once TRIGGER is pressed the output will rise to 100V and reach a peak output current of 17A, likely destroying M1 and M2.

Do not apply the output to a shunt clamp, such as to produce ISO 7637-2 test pulse 5b. Doing so will result in a contest between the high voltage power supply, M1 and M2, and the shunt clamp.

Do not operate under load without the low voltage supply (12V INPUT) powered up to at least 10.7V. Doing so exposes M1 and M2 to a much longer pulse width than normal, causing potentially destructive SOA stress.

Do not operate DC1950A without the ground (GND) terminal connected to the ground of the power supplies and DUT. Doing so will cause the output to rise to the high voltage supply and stay there for 8 seconds.

Do not operate DC1950A with the cover removed. Everything inside the box floats on the source of MOSFET M1, and rises to the high voltage input when the TRIGGER push button is pressed. In particular, the MOSFET heat sinks are connected to the high voltage supply (107V INPUT) and always represent a shock hazard.

Do not connect a ground to anything inside DC1950A. See the previous paragraph.

## QUICK START PROCEDURE

### Overview

DC1950A generates ISO 7637-2 test pulse 5a. Two supplies are required: one for the normal operating voltage (12V INPUT, nominally 14.2V or 27.7V) and a second for the load dump pulse which rises to within 5V of the 107V INPUT terminal. Each supply may be varied to test the load under a variety of operating conditions. Diodes are included to block back feeding from one supply to the other. Note that the DC output voltage is 0.7V less than that applied to the 12V INPUT.

An especially rugged MOSFET specifically designed for saturated operation has been selected for the pass element: the IXYS IXTX90N25L2, representing the best-in-class MOSFET with a generous, reliably characterized safe operating area. Two of these devices are operated in parallel.

The MOSFETs are mounted on small heat sinks which serve as thermal masses to reduce junction temperature rise and help radiate energy absorbed by the MOSFETs.

A block diagram of DC1950A is shown in Figure 1. A flip flop configured as a one shot is powered by two 9V batteries, BT1 and BT2. The flip flop floats and its reference common is connected to the source of M1. When the TRIGGER push button S1 is pressed, the flip flop is set and its Q output charges C4 through R9. The flip flop is reset when the source of M1 approaches to within about 5V of the 107V INPUT. C4 is then discharged by R22, producing an exponential decay. R21 accelerates the discharge rate as a function of load current, while M1 and M2 simply buffer the C4 waveform to drive the output.

R17 and R18 serve two purposes. First, they establish a 2Ω generator resistance (called “Ri” in the ISO 7637-2 specification). Second, they ballast M1 and M2 to help equalize their drain currents.

D7 and D8 serve to OR the load dump pulse with the 12V INPUT voltage, thereby preventing any chance of back feeding one supply into the other.

To summarize, a load dump pulse is initiated by pressing the TRIGGER push button. The peak output voltage rises to within about 5V of the voltage applied to the 107V INPUT terminal, and the timing is controlled by C4, R21 and R22. The flip flop floats and rides on the source of M1. There is no on/off switch because the flip flop circuit draws no static (DC) current from the batteries.

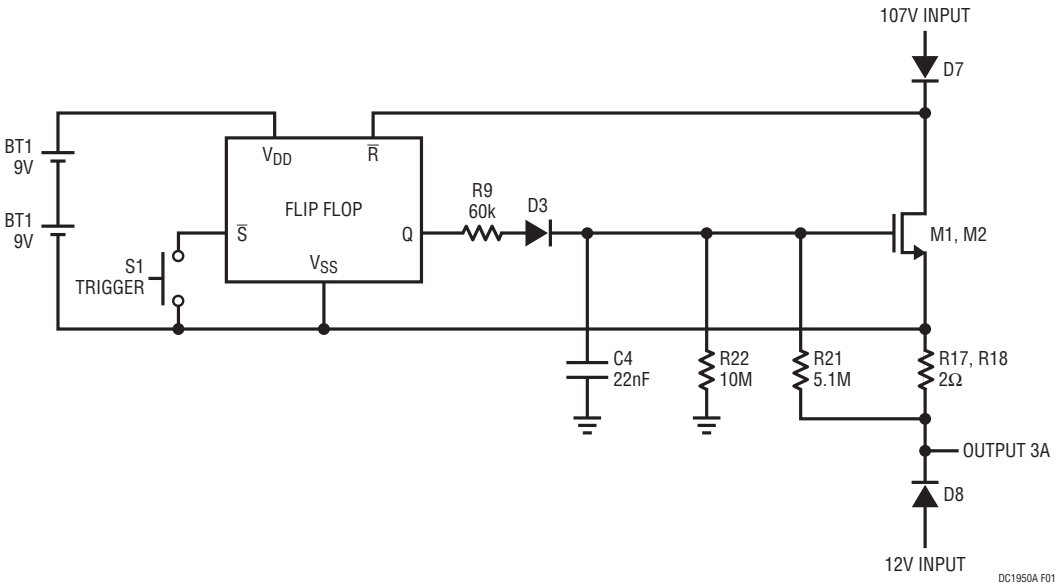


**Figure 1. Block Diagram**

## QUICK START PROCEDURE

### Detailed Circuit Description

Refer to the schematic diagram. Switch S1 is debounced by a flip flop, comprising U1A, U1B, R3 and C2, and is subject to a lengthy 8 seconds debounce lockout period by the charging and discharging action of R3 and C2. The flip flop is set by closing S1, and a debounced rising edge appears at U1D's output just three propagation delays later.

C2 charges while the flip flop is set. During this interval repeated closures of S1 have no effect because they simply reinforce the fact that the flip flop is already set. When C2 reaches 2/3 supply, U1C trips and blocks further closures of S1 by holding the flip flop in reset, and by forcing U1D's output to remain high. When C2 discharges to 1/3 supply U1C returns U1D's output low and releases the flip flop reset input so that it can once again recognize closures of S1.

If S1 closes while the flip flop is held in reset, U1A's output goes high and causes C2 to recharge for as long as S1 is closed. This forestalls C2's inevitable discharge and lengthens the effective lockout period, but no edge is issued from U1D's output. S1 must be released long enough for C2 to discharge to 1/3 supply before an S1 closure is once again recognized and propagated to U1D's output.

The rising edge of U1D's output (which was instigated by the initial closure of S1) triggers a 1µs one shot comprising U2A and U2B. The negative-going output pulse from U2B triggers a final flip flop formed by U2C and U2D. The output of U2C goes high five propagation delays after S1 is pressed, charging C4 and the MOSFET gates through R9.

Initially the MOSFETs are off; their gates are held slightly below source potential by Q1. After a delay of about 1ms, the gates of M1 and M2 reach threshold and the source terminals begin to follow. The voltage across R9 is approximately constant (18V–$V_{GSTH}$), $C_{GS}$ is bootstrapped, and the charging current flows in C4 and $C_{RSS}$. To a first order the charging current is constant (perhaps 220µA) and the capacitance is constant (C4 + 2$C_{RSS}$), so the output ramps linearly at a rate of 100V in 10ms.

$C_{RSS}$ is for the most part negligible, but also highly variable. In particular as $V_{DS}$ collapses towards zero, $C_{RSS}$ rises dramatically. This effect causes a small but sometimes visible distortion to the output waveform as it reaches its peak.

As the source of M1 nears the 107V INPUT, D2 pulls down and resets U2C and U2D. The output of U2C goes low and stops charging C4. C4 is then discharged by resistor R22. If the output is heavily loaded a voltage appears across R17 and R18, which produces an additional discharge current in R21 and accelerates the falling edge. R21 and R22 are buffered by common base amplifier Q1 to eliminate a small residual error arising from $V_{GSTH}$ and thereby preserve the exponential discharge characteristic and timing.

Rather than relying on Q1 to hold M1 and M2 off such as during long term storage, the output of U1D is fed forward through R7 and D4 to pull the gates of M1 and M2 low after the debounce time. For this reason the debounce time must be longer than the load dump pulse, otherwise the output will collapse before the pulse is complete.

A few other components may arouse the interest of the curious. D1 is included to protect against reverse battery, and to also block charging current in the event a MOSFET failure leads to back feeding of the 18V rail. Since U1 and U2 are operated at near their maximum rating of 18V, R1 is included to suppress any ringing that might arise from connecting the batteries. D5 and D6 guard against unforeseen gate voltage excursions beyond 18V, R15 and R16 average the source voltages for the benefit of Q1, and R19 and R20 provide a small DC path to keep D8 biased and to provide a discharge path for the load dump pulse under conditions of no load. Snubbers stabilize M1 and M2 to prevent parasitic oscillations.

## QUICK START PROCEDURE

### Modifications

Output pulse timing may be trimmed by adjusting R9 (rise time) and R23 (fall time). The rising slew rate can be adjusted over a range of 5V/ms to 50V/ms to suit various requirements. The falling time constant is set to approximate a pulse width of 400ms, unloaded, and can be adjusted ±10%. Note that the ISO fall time specification is not the waveform exponential time constant, but rather the time from the start of the pulse to 10% of the peak delta surge amplitude.

Gross output pulse timing is controlled by C4 at roughly 18s/µF. C4A is stuffed with 22nF and C4B is left open. Through-hole pads are provided for adding a selector switch or fixed, leaded capacitor. It is possible to produce pulses of up to many seconds in length, although dissipation in M1 and M2 will severely limit the output current capability for long pulses.

The recommended C4 voltage rating is 250V for film and 500V for ceramic. If C4 is removed, timing is controlled by $C_{RSS}$ which produces a pulse width of perhaps 50ms to 100ms. The waveform will show obvious distortion owing to the strong voltage dependence of $C_{RSS}$. Even with C4 = 22nF, some distortion of the exponential is visible to the discerning eye at the peak of the output pulse. For this reason pulse intervals of less than 200ms are discouraged.

The push button is debounced by a flip flop. Once the circuit is triggered, all subsequent button presses are ignored until C2 has discharged to 1/3 supply. The debounce period is approximately 1.8s/µF, or 8 seconds for C2 = 4.7µF. Change C2 to alter the debounce time. To ensure the debounce time is longer than the pulse time, keep C2 ≥ 10•C4.

The generator resistance, Ri, is equal to the parallel combination of R17 and R18. These may be changed to alter Ri. For example to achieve an Ri of 10Ω, change R17 and R18 to 20Ω each.

## QUICK START PROCEDURE

### How to Operate DC1950A

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A basic connection diagram is shown in Figure 2. First power up the low voltage supply (14.2V connected to 12V INPUT) and adjust for the correct output voltage at the DUT. Keep in mind that there is a diode between 12V INPUT and OUTPUT 3A.

Once proper operation of the DUT has been verified, power up the high voltage supply (107V connected to the 107V INPUT) and press the TRIGGER push button. After the pulse is complete, turn off the high voltage supply.

In a typical test setup the DUT input voltage and current are measured, while the two remaining oscilloscope channels are used initially to monitor the low and high voltage supplies, making certain they do not collapse, overshoot or otherwise misbehave as a result of some transient operating condition. Once proper test setup behavior is verified, the latter two channels can be transferred to the DUT to observe its operating behavior during a load dump pulse event.

For 24V operation, the rise time will approximately double, yet the ISO specification calls for the same 10ms open circuit rise time as the 12V spec. If this minor difference is important, adjust R9 for an open circuit rise time of 10ms.

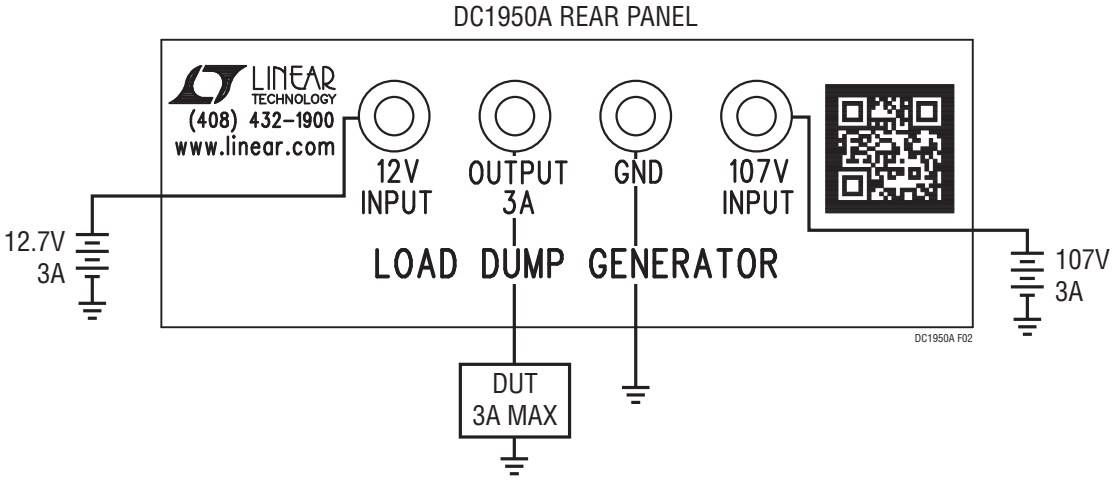


**Figure 2. Basic Load Dump Test Setup**

## QUICK START PROCEDURE

### Battery Installation

To install batteries BT1 and BT2, remove the two #1 Phillips machine screws in the bottom cover. Next remove the top cover, followed by the front panel containing the TRIGGER push button switch to gain better access to the battery holders. Install the batteries, replace the front panel and reassemble the case.

Because battery life is limited by shelf life, there is a much greater risk of damage arising from battery leakage than from low battery circuit malfunction. For this reason, write the date of battery installation on the rear panel with a permanent felt tip pen, as a reminder of when to change the batteries. Batteries should be changed annually or simply removed during long intervals of disuse. "Permanent" felt tip pen markings are easily removed with 2-propanol.

### Load Dump Pulse Behavior

The ISO 7637-2 load dump pulse is a codification of the internal specifications of numerous automotive manufacturers. Most, if not all, major manufacturers have their own load dump pulse specification which, if not identical to, closely resembles the prototypical ISO waveform in shape and behavior. In addition, any of numerous standards organizations publish similar pulse specifications. Because ISO 7637-2 test pulse 5a is representative of the vast majority of these specifications, DC1950A needs no adjustment or modification. R9 and R23 are provided to permit trimming and adjustment to match those that fall outside of the ISO envelope. Where the departure is major, C4 is used to make adjustments.

There are two important facts to understand about a load dump pulse as defined by ISO 7637-2. First, generator resistance Ri affects the shape of the waveform applied to the DUT. The prototypical waveform exists at the output of the generator, but the OUTPUT 3A terminal is on the other side of a 2Ω resistor. Current flow in the DUT, dropped across 2Ω, directly subtracts from the generator voltage. For this reason it is important to monitor the input current with a DC coupled current probe to quickly ascertain the cause of any anomalies in the DUT voltage waveform.

A second, equally important fact is that the time constant of the falling edge is a function of load current. If the output is unloaded, the time to 10% is 400ms; if loaded with 2Ω (not recommended as it will destroy the MOSFETs), the time to 10% shortens to 200ms.

Thus there are two factors contributing to departures from an open circuit 400ms exponential decay at the output, generator resistance Ri and fall time acceleration. Do not expect the peak loaded output waveform to reach 99V or to show a textbook exponential decay. One last factor that may affect the pulse waveform is voltage regulation of the power supplies. When in doubt, monitor both power supplies.

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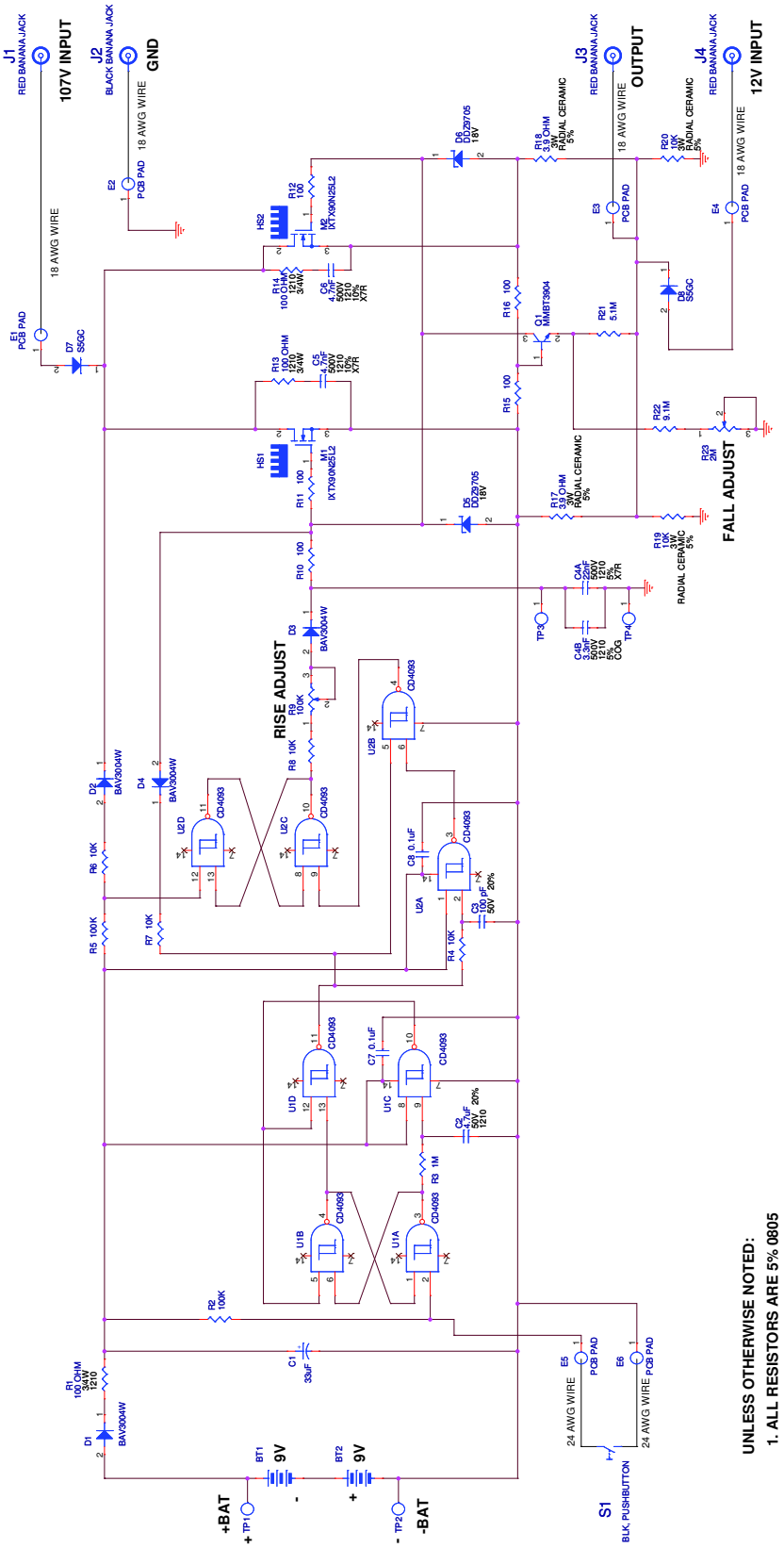
## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|---|---|---|---|---|
| 1 | 2 | BT1, BT2 | 9V BATTERY HOLDER, METAL | KEYSTONE, #1290 |
| 2 | 1 | C1 | CAP., ALUM., 33µF 50V 20% SMT | SUN ELECT., 50CE33LX |
| 3 | 1 | C2 | CAP., X7R, 4.7µF, 50V 20% 1210 | AVX, 12105C475MAT2A |
| 4 | 1 | C3 | CAP., X7R, 100pF, 50V 20% 0805 | AVX, 08055C101MAT4A |
| 5 | 1 | C4A | CAP., X7R, 22nF, 500V 5% 1210 | AVX, 12107C223JAT2A |
| 6 | 0 | C4B (OPT) | CAP., COG, 3.3nF, 500V 10% 1210 | KEMET, C1210C333KCRACTU |
| 7 | 2 | C5, C6 | CAP., X7R, 4.7nF, 500V 10% 1210 | AVX, 12107C472KAT2A |
| 8 | 2 | C7, C8 | CAP., X7R, 0.1µF, 50V 20% 0805 | AVX, 08055C104MAT2A |
| 9 | 4 | D1, D2, D3, D4 | DIODE, SWITCH 300V 400MW SOD123 | DIODES INC., BAV3004W-7-F |
| 10 | 2 | D5, D6 | DIODE, ZENER 18V 500mW SOD-123 | DIODES INC., DDZ9705-7 |
| 11 | 2 | D7, D8 | DIODE, GEN PURPOSE 400V 5A SMC | DIODES INC., S5GC-13-F |
| 12 | 2 | HS1, HS2 | HEATSINK, TO-247, CLIP-ON BLK | OHMITE, WA-T247-101E |
| 13 | 3 | J1, J3, J4 | CONN., JACK BANANA INSUL NYLON RED | EMERSON NETWORK,108-0902-001 |
| 14 | 1 | J2 | CONN JACK BANANA INSUL NYLON BLA | EMERSON NETWORK,108-0903-001 |
| 15 | 2 | M1, M2 | MOSFET, N-CHANNEL 90A 250V PLUS247 | IXYS, IXTX90N25L2 |
| 16 | 1 | Q1 | TRANSISTOR, GP, 40V, 200mA, SOT-23 | ON SEMI., MMBT3904LT1G |
| 17 | 3 | R1, R13, R14 | RES., CHIP, H-POWER, 100Ω, 3/4W, 5% 1210 | VISHAY, CRCW1210100RJNEAHP |
| 18 | 2 | R2, R5 | RES., CHIP, 100k, 1/8W, 5% 0805 | VISHAY, CRCW0805100KJNEA |
| 19 | 1 | R3 | RES., CHIP, 1M, 1/8W, 5% 0805 | VISHAY, CRCW08051M00JNEA |
| 20 | 4 | R4, R6, R7, R8 | RES., CHIP, 10k, 1/8W 5% 0805 | VISHAY, CRCW080510K0JNEA |
| 21 | 1 | R9 | TRIMMER, 100k, 0.5W CERMET PC PIN | BOURNS, 3386P-1-104LF |
| 22 | 5 | R10-R12, R15, R16 | RES., CHIP, 100Ω, 1/8W, 5% 0805 | VISHAY, CRCW0805100RJNEA |
| 23 | 2 | R17, R18 | RESISTOR CER 3.9Ω 3W RADIAL 5% WIREWOUND | OHMITE, TWW3J3R9E |
| 24 | 2 | R19, R20 | RES., RADIAL CERAMIC, 10k, METAL OXIDE | OHMITE, TWM3J10KE |
| 25 | 1 | R21 | RES., CHIP, 5.1M, 1/4W, 5% 1206 | VISHAY, CRCW120655M10JNEA |
| 26 | 1 | R22 | RES., CHIP, 9.1M, 1/4W, 5% 1206 | VISHAY, CRCW012069M10JNEA |
| 27 | 1 | R23 | TRIMPOT, 2M, CERMET, PC PINS, SINGLE TURN | BOURNS, 3386P-1-205LF |
| 28 | 1 | S1 | SWITCH, PUSHBUTTON, MOMENTARY N.O., PANEL MOUNT | E-SWITCH, RP3502ABLK |
| 29 | 2 | U1, U2 | IC., QUAD NAND GATE, CMOS, 14-SOIC | TEXAS INSTRUMENTS, CD4093BM96 |
| 30 | 1 | | ENCLOSURE, BOX, ABS 5.29 × 5, 0.32 × 2 .01" BLACK | HAMMOND MFG., 1598BBK |
| 31 | 2 | | BATTERY, 9V, ALKALINE | ENERGIZER BAT. CO., EN22 |

## SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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